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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
THOMAS, ERIC W	

ART UNIT	PAPER NUMBER
2831	

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/826,605	PRYMAK, JOHN D.	
	Examiner	Art Unit	
	Eric W Thomas	2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-56* is/are pending in the application.

4a) Of the above claim(s) *30-45* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29 and 46-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/9/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-29, 46-56, drawn to a capacitor, classified in class 361, subclass 309.

II. Claims 30-45, drawn to a method of forming a capacitor, classified in class 29, subclass 25.42.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claim does not require the dielectric to be formed from a green sheet; the product can be cured; and the process can form a resistive element.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Mr. Joseph Guy on 12/17/04 a provisional election was made WITH traverse to prosecute the invention of I, claims 1-29, 46-56. Affirmation of this election must be made by applicant in replying to this Office action. Claims 30-45 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 26-29, 56 are rejected under 35 U.S.C. 102(e) as being anticipated by Sutardja (US 2004/0223290).

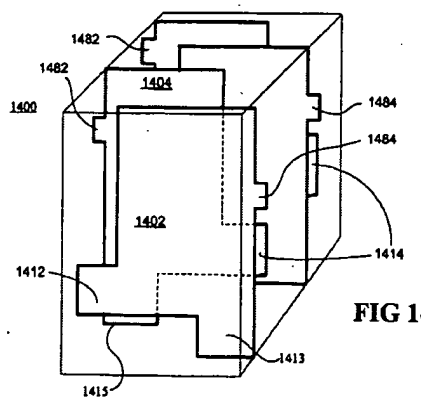


FIG 14A

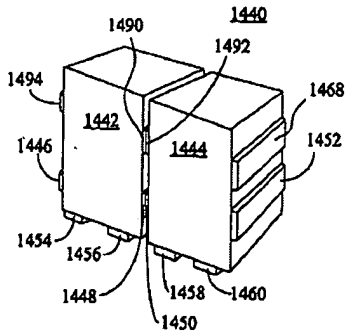


FIG 14B

Sutardja discloses in fig. 14A, 14B, a capacitor comprising: a first face and a second face parallel to said first face and four sides perpendicular to and between said first face and said second face; subunits (1442, 1444) wherein each subunit of said subunits comprises: first plates (1402) and second plates (1404) in alternating planar relationship with a dielectric (paragraph 39) therebetween; each first plate of said first plates comprises a first coupling tab and a power tab (see 12a, 12b – polarity) on opposing edges wherein said first coupling tab terminates at said first face and said

power tab terminates at said second face; each second plate of said second plates comprises a second coupling tab and a ground tab on opposing edges wherein said second coupling tab terminates at said first face and said ground tab terminates at said second face.

Regarding claim 27, Sutardja discloses a ceramic is between the subunits (from each laminated subunit).

Regarding claim 28, Sutardja discloses the first coupling tabs of each subunit are aligned.

Regarding claim 29, Sutardja discloses the first coupling of each subunit and said second coupling of each subunit are alternating.

Regarding claim 56, Sutardja discloses a capacitor for attachment to a printed circuit board comprising a multiplicity of termination contacts along a face, which is parallel with said printed circuit board; said termination points are arranged in an interdigitated fashion such that adjacent, internal electrode plates are terminated to opposite contacts and non-adjacent plates, wherein every other plate, is terminated to like termination points.

3. Claims 46-55 are rejected under 35 U.S.C. 102(e) as being anticipated by Vieweg et al. (US 2004/0125540).

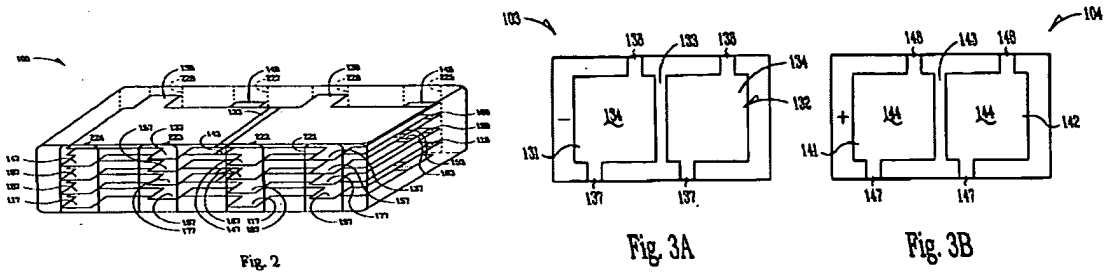


Fig. 2 Fig. 3A Fig. 3B

Vieweg et al. disclose in fig. 2, 3A, 3B, a capacitor comprising: a pair of opposing faces; subunits wherein each subunit comprises a multiplicity of first plates and second plates alternating parallel relationship and perpendicular to said opposing faces; said first electrodes comprise first lead out tabs (137, 177; 137, 177) which terminate at a first external terminal at a first face; said second electrodes comprise second lead out tabs (147, 187; 147, 187) which terminate at a second external terminal at said first face; a first external terminal (223; 221) in contact said first lead out tabs; a second external terminal (222, 224) in contact with said second lead out tabs; said subunits are arranged in parallel such that said first external terminals and said second external terminals are on said first face.

Regarding claim 47, Vieweg et al. disclose said first external terminal of each said subunit are aligned.

Regarding claim 48, Vieweg et al. disclose said first external terminal is in electrical contact with a first external terminal of a second said subunit.

Regarding claim 49, Vieweg et al. disclose said first external terminal of each said subunit and said second external terminal of each said subunit are alternating.

Regarding claim 50, Vieweg et al. (as seen in fig. 2) disclose each of said first plates comprises third lead out tabs (138; 138) which terminate at a third external terminal (228, 226) on a second face.

Regarding claim 51, Vieweg et al. (as seen in fig. 2) disclose each of said second plates comprises fourth lead out tabs (148; 148) which terminate at a fourth external terminal (225, 227) on said second face.

Regarding claim 52, Vieweg et al. (as seen in fig. 2) disclose said third external terminal and said fourth external terminal are aligned.

Regarding claim 53, Vieweg et al. disclose said third external terminal and said fourth external terminal are alternating (as seen in fig. 2).

Regarding claim 54, Vieweg et al. disclose said first external terminal and said third external terminal are opposing.

Regarding claim 55, Vieweg et al. disclose said first external terminal and said fourth external terminal are opposing.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4, 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahiko et al. (US 6,292,351) in view of Vinson et al. (US 6,700,794).

FIG. 1

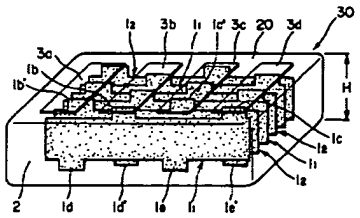


FIG. 2

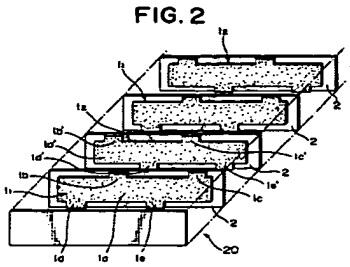
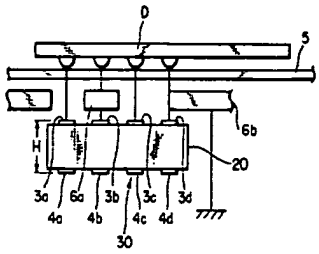


FIG. 4



Ahiko et al. disclose in fig. 1-4, an electrical component comprising: a printed circuit board (5) comprising an upper face and a lower face a semiconductor (D) mounted to said upper face; a capacitor (20) mounted to said lower face wherein said capacitor comprises: a first face parallel to said printed circuit board and a second face opposite to said first face; first plates (1_1) and second plates (1_2) in alternating planar relationship with a dielectric (2) therebetween; each first plate of said first plates comprises a first coupling tab and a power tab on opposing edges wherein said first coupling tab terminates at said first face and said power tab terminates at said second face; each second plate of said second plates comprises a second coupling tab and a ground tab on opposing edges wherein said second coupling tab terminates at said first face and said ground tab terminates at said second face; wherein said first coupling tab and said second coupling tab are in electrical contact with said semiconductor.

Ahiko et al. disclose the claimed invention except of the semiconductor is a microprocessor.

Vinson et al. teach that it is known in the art to form high-speed digital integrated circuit microprocessors and memories formed as a semiconductor die (as seen in col. 1 lines 10-20). It would have been obvious to a person of ordinary skill in the art at the

time the invention was made to use the high-speed digital integrated circuit microprocessor as taught by Vinson et al in the system of Ahiko et al., since such a modification would provide a microprocessor for the system of Ahiko et al. having a high-speed.

Regarding claim 2, Ahiko et al. disclose each said first plate comprises a multiplicity of power tabs and a multiplicity of first coupling tabs.

Regarding claim 3, Ahiko et al. disclose each power tab terminates at said second face.

Regarding claim 4, Ahiko et al. disclose the first plates and said second plates are substantially perpendicular to said printed circuit board.

Regarding claim 11, Ahiko et al. disclose the first coupling tab and the power tab are opposing.

Regarding claim 12, the modified Ahiko et al. disclose an electrical component comprising: a printed circuit board comprising an upper face and a lower face a microprocessor mounted to said upper face; a subunit mounted to said lower face wherein said subunit comprises a first face parallel to said printed circuit board and a second face opposite to said first face; first plates and second plates in alternating planar relationship with a dielectric therebetween; each first plate of said first plates comprises a first coupling tab and a power tab on opposing edges wherein said first coupling tab terminates at said first face and said power tab terminates at said second face; each second plate of said second plates comprises a second coupling tab and a ground tab on opposing edges wherein said second coupling tab terminates at said first

face and said ground tab terminates at said second face; wherein said first coupling tab and said second coupling tab are in electrical contact with said microprocessor.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahiko et al. (US 6,292,351) and Vinson et al. (US 6,700,794) as applied to claim 1 above, and further in view of JP 2001-255954 ('954).

Ahiko et al. discloses the claimed invention except for the capacitor is attached to a printed circuit board using a solder strip.

'954 illustrates in fig. 6, that forming a connection using a solder strip is know in the art. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a solder strip to connect the capacitor to the printed circuit board, since such a modification would provide a means to connect the capacitor to the printed circuit board, and would allow the external terminals of the capacitor to connect to specific electrical paths.

7. Claims 1, 5-8, 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vieweg et al. (US 2004/0125540) in view of Nakaya et al. (US 4,982,485) and Vinson et al. (US 6,700,794)

Vieweg et al. disclose a capacitor comprising a first face and a second face opposite to said first face; first plates and second plates in alternating planar relationship with a dielectric therebetween; each first plate of said first plates comprises a first coupling tab and a power tab on opposing edges wherein said first coupling tab terminates at said first face and said power tab terminates at said second face; each second plate of said second plates comprises a second coupling tab and a ground tab

on opposing edges wherein said second coupling tab terminates at said first face and said ground tab terminates at said second face. The capacitor is connected to a substrate (509) and a processor (503 – "processor" – paragraph 27) is connected to the substrate.

Vieweg et al. disclose the claimed invention except the processor die is a microprocessor and the substrate is a printed circuit board.

Nakaya et al. teach that a printed circuit board is a substrate known in the art.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a printed circuit board as the substrate in the system of Vieweg et al., since such a modification would allow multiple passive components, interconnects, and other components to be formed in the system.

Vinson et al. teach that microprocessors are known in the art.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a "microprocessor" in the system of Vieweg et al., since such a modification would provide a processor that has is small.

Regarding claim 5, Vieweg et al. dislcose the capacitor comprises subunits wherein each subunit comprises first coupling tabs, second coupling tabs, power tabs and ground tabs.

Regarding claim 6, Vieweg et al. disclose comprising first external coupling terminations in electrical contact with said first coupling tabs and second external coupling terminations in electrical contact with said second coupling tabs.

Regarding claim 7, Vieweg et al. disclose said first external coupling terminations are linearly coupled.

Regarding claim 8, Vieweg et al. disclose said first external coupling terminations and said second external coupling terminations are alternating.

Regarding claim 9, Vieweg et al. disclose the capacitor is attached to the printed circuit board by a ball grid array (see paragraph 28).

Regarding claim 12, Vieweg et al. disclose an electrical system comprising a substrate (509) comprising an upper face and a lower face, a processor (503) mounted to the upper face capacitor comprising first and second face opposite each other; first and second plates in alternating planar relationship with a dielectric material therebetween, each first plate comprising a first coupling tab and a power tab on opposing edges wherein the first coupling tab terminates at the first face and the power tab terminations at said second face; each second plate of the second plates comprise a second coupling tab and a ground tab on opposite edges wherein the second coupling tab terminates at the first face and the ground tab terminates at a second face; wherein the first coupling tabs and the second coupling tabs are in electrical contact with the processor.

Vieweg et al. disclose the claimed invention except the processor die is a microprocessor and the substrate is a printed circuit board.

Nakaya et al. teach that a printed circuit board is a substrate known in the art.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a printed circuit board as the substrate in the system of

Vieweg et al., since such a modification would allow multiple passive components, interconnects, and other components to be formed in the system.

Vinson et al. teach that microprocessors are known in the art.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a "microprocessor" in the system of Vieweg et al., since such a modification would provide a processor the is small in size.

Regarding claim 13, Vieweg et al. disclose the electrical component comprises multiple subunits.

Regarding claim 14, Vieweg et al. disclose said subunits are combined to form a capacitor.

Regarding claim 15, Vieweg et al. disclose said capacitor comprises ceramic (133, 143, 173, 183) between said subunits.

Regarding claim 16, Vieweg et al. disclose said first coupling tabs of each subunit are aligned.

Regarding claim 17, Vieweg et al. disclose said first coupling of each subunit and said second coupling of each subunit are alternating.

8. Claims 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vieweg et al. (US 2004/0125540) in view of Vinson et al. (US 6,700,794).

Regarding claim 18, Vieweg et al. disclose an electrical component comprising a substrate comprising power terminals and ground terminals (not shown – see paragraph 28); a capacitor (100) mounted on the substrate wherein the capacitor comprises alternating first plates and second plates with a dielectric between said first plates and

second plates wherein said first plates and said second plates are perpendicular to said printed circuit board; wherein said first plates comprise power lead out tabs terminating at power external terminals and coupling lead out tabs terminating at first coupling terminals wherein said power external terminals are in electrical contact with said power terminals; and said second plates comprise ground tabs terminating at ground external terminals and second coupling tabs terminating at second coupling terminals wherein said ground external terminals are in electrical contact with said ground terminals; a substrate (515) with said capacitor mounted thereon comprising power coupling terminals (not shown see paragraph 28) in electrical contact with said first coupling terminal and ground coupling terminals in electrical contact with said second coupling terminals.

Vieweg et al. disclose the claimed invention except for the substrates are a printed circuit board/chipboard.

Nakaya et al. teach that a printed circuit board/chipboard is a substrate known in the art.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a printed circuit board/chipboard as the substrate in the system of Vieweg et al., since such a modification would allow multiple passive components, interconnects, and other components to be formed in the system.

Regarding claim 19, Vieweg et al. disclose said power lead out tabs and said ground tabs are in alternating arrangement.

Regarding claim 20, Vieweg et al. disclose the capacitor is mounted to said printed circuit board by a ball grid array (paragraph 28).

Regarding claim 21, Vieweg et al. disclose said power lead out tabs are aligned and said ground tabs are aligned.

9. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vieweg et al. (US 2004/0125540) and Vinson et al. (US 6,700,794) as applied to claim 21 above, and further in view of JP 2001-255954 ('954).

Vieweg et al. disclose the claimed invention except for the capacitor is mounted to the printed circuit board by a solder strip. Vieweg et al. discloses in paragraph 28, that the capacitor is connected to the substrate by surface mount connections.

'954 illustrates in fig. 6, that forming a connection using a solder strip is know in the art. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a solder strip to connect the capacitor to the printed circuit board, since such a modification would provide a means to connect the capacitor to the printed circuit board, and would allow the external terminals of the capacitor to connect to specific electrical paths.

10. Claims 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vieweg et al. (US 2004/0125540) and Vinson et al. (US 6,700,794) as applied to claim 18 above, and further in view of Vinson et al. (US 6,700,794).

Vieweg et al. disclose a processor is mounted on the printed circuit board. Vieweg et al. disclose the claimed invention except for the processor is a microprocessor.

Vinson et al. teach that microprocessors are known in the art.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a "microprocessor" in the system of Vieweg et al., since such a modification would provide a processor that is small.

Regarding claim 24, Vieweg et al. disclose the substrate (printed circuit board) is between the capacitor and the processor (microprocessor).

11. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vieweg et al. (US 2004/0125540) and Vinson et al. (US 6,700,794) as applied to claim 18 above, and further in view of Menzies et al. (US 5,982,635).

Vieweg et al. disclose the claimed invention except for the electrical component comprising a heat sink.

Menzies et al. teach that it is known in the art to use a heat sink with an electrical component.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a heat sink in the electrical component of Vieweg et al, since such a modification would assist in cooling the electrical component.

Conclusion

In order to ensure full consideration of any amendments, affidavits, or declaration, or other documents as evidence of patentability, such documents must be submitted in response to this Office action. Submissions after the next Office action, which is intended to be a final action, will be governed by the requirements of 37 CFR 1. 116 which will be strictly enforced.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric W Thomas whose telephone number is 571-272-1985. The examiner can normally be reached on M,Tu,Sat 9 am - 9:30 pm; W, Th, F 6 pm -10:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eric W Thomas
Examiner
Art Unit 2831

ewt